REMARKS

Applicant respectfully requests reconsideration of the subject application as amended. In response to the Office Action mailed 6/15/05, Applicant is filing an RCE with this response. Claims 1-6, 9-16, 19 and 20 are still pending.

In the Office Action mailed 6/15/05, the Examiner has rejected claims 1 and 3-5 under 35 U.S.C. §102(b) as being anticipated by Avnon et al. (U.S. Patent 5,559,977; "Avnon") and applied the same rejection to other claims as well, based on similarities of those claims to claims 1 and 3-5. Furthermore, the Examiner has rejected claims 2, 9-10, 12 and 19 under 35 U.S.C. §103(a) as being unpatentable over Avnon in view of the Patterson et al. article and rejected claims 6 and 16 over Avnon in view of Halfill ("SiByte Reveals 64-Bit Core for NPUs").

In reply, Applicant submits that Avnon fails to disclose the claimed embodiments of the invention, whether alone or combined with Patterson et al. and/or Halfill. The Examiner has noted a number of lines of text in Avnon in presenting his reasons for rejecting the pending claims. However, the teachings of Avnon pertain to a single pipeline structure. For example, Figure 3 of Avnon illustrates four stages of a pipeline for integer instructions handling, so that "instruction pairs (i.e., IP1-4) being executed in the D1, D2, E and WB stage in synchronization" (Avnon at col. 7, lines 22-23). The floating-point pipeline "shares the first four stages with the integer pipeline and then continues with four more stages: X1, X2, WF and ER" (Avnon at col. 7, lines 35-38). In Figure 4 of Avnon, "IP1 and IP2 are floating-point instructions while IP3 and IP4 are integer instruction pairs" (Avnon at col. 7, lines 50-51).

Furthermore, Avnon teaches that "[i]f an exception is possible on a single floating-point instruction, the floating-point pipeline of Fig. 4 stalls subsequent floating-point instructions in the E stage until a determination is made that the instruction actually does not generate an exception. If an exception is possible on a pair of floating point instructions that were issued together, subsequent integer instructions are stalled in the D2 stage, while subsequent floating-point instructions are stalled in the E stage of the pipeline" (Avnon at col. 8, lines 2-10). Furthermore, "[i]f there is a single or pair of

floating-point instructions that are determined to be unsafe in the floating-point pipeline, FIRC 201 stalls the subsequent floating-point microinstruction at the E stage in the pipeline" (Avnon at col. 9, lines 16-19). "[I]f a floating-point instruction pair is issued, FIRC 201 stalls the integer execution pipeline at the D2 stage" (Avnon at col. 9, lines 24-25), but "if a single floating-point instruction is labeled unsafe, the integer pipeline need not stall" (Avnon at col. 9, lines 34-35).

Applicant submits that the claimed embodiments of the invention pertain to multiple pipelines (first and second pipelines in claim 1) and not to a single shared pipeline. With multiple pipelines, an instruction to the pipeline with less stages is inhibited from co-issuing to that pipeline. This applies to a single floating-point instruction being issued to the pipeline having greater number of stages, in which co-issuing of an instruction to the shorter pipeline is inhibited. Applicant submits that these aspects of the invention as claimed in the independent claims are not disclosed by Avnon or any of the other relied upon references.

Accordingly, Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. §102(b) and 35 U.S.C. §103(a) rejections and allow pending claims 1-6, 9-16, 19 and 20.

If there are any fee shortages related to this response, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

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